Amendments to the Claims:

Please amend claims 21, 31 and 42. Please add new claims 43-48. The claims are as follows:

1–20 (Canceled)

21. (Currently Amended) An electrical structure, comprising:

a parent terrain denoted as V_0; ~~and~~

voltage islands denoted as V_1 and V_2, said voltage island V_1 nested within said parent terrain V_0 and said voltage island V_2 nested within said voltage island V_1; and

a logic circuit voltage power supply connected to a logic circuit and an externally supplied state saving power supply connected to a logic state saving circuit, said logic circuit and said state saving circuit within either said voltage island V_1 or said voltage island V_2.

22. (Previously Presented) The electrical structure of claim 41, wherein each voltage island of the N voltage islands includes one or more voltage power supplies selected from the group consisting of an internal voltage island VDDI power supply, an externally supplied state saving VDDSS power supply, an externally supplied VDDN power supply, and combinations thereof.

23. (Previously Presented) The electrical structure of claim 22, wherein said one or more power supplies of voltage island V_X for X=1, 2,…, N are each independently coupled to one of (a) said one or more power supplies of voltage island V_Y, for Y=1, 2,…, N, X not equal to Y, (b) a VDDO power supply of said parent terrain or (c) one or more external to said parent terrain power supplies.

24. (Previously Presented) The electrical structure of claim 41, wherein each voltage island of the N voltage islands includes (a) an externally supplied VDDN power supply and a voltage shifting means, or (b) said externally supplied VDDN power supply and a fencing means, or (c) said externally supplied VDDN power supply, said voltage shifting means and said fencing means.

25. (Previously Presented) The electrical structure of claim 24, wherein said fencing means comprises logic latches.

26. (Previously Presented) The electrical structure of claim 24, wherein each voltage island of the N voltage islands further includes one or more substructures selected from the group consisting of (a) an internal voltage island VDDI power distribution network, (b) state saving means, (c) one or more switching elements coupled between said externally supplied VDDN power supply and said internal voltage island VDDI power distribution network, and (d) one or more voltage buffering circuits.

27. (Previously Presented) The electrical structure of claim 26, wherein said one or more switching elements is selected from the group consisting of hard connections, voltage regulators, headers and footers.

28. (Previously Presented) The electrical structure of claim 26, wherein said state saving means includes at least one state saving latch.

29. (Previously Presented) The electrical structure of claim 41, wherein one or more voltage islands of the N voltage islands further includes a power management state machine coupled to an internal voltage island VDDI power supply distribution network, said power management state machine of voltage island V_X for X=1, 2,…, N located in (a) voltage island V_Y for Y=1, 2,…, N, Y less than X, or (b) in said parent terrain.

30. (Previously Presented) The electrical structure of claim 21, wherein said parent terrain is an integrated circuit chip or a voltage island within said integrated circuit chip.

31. (Currently Amended) A method, comprising:

providing a parent terrain denoted as V_0; ~~and~~

nesting a voltage island V_1 within said parent terrain V_0 and nesting a voltage island V_2 within said voltage island V_1; and

providing a logic circuit voltage power supply to logic circuits and providing and an externally supplied state saving power supply to logic state saving circuits, said logic circuit and said state saving circuit within either said voltage island V_1 or said voltage island V_2.

32. (Previously Presented) The method of claim 42, wherein each voltage island of the N voltage islands includes one or more voltage power supplies selected from the group consisting of an internal voltage island VDDI power supply, an externally supplied state saving VDDSS power supply, an externally supplied VDDN power supply, and combinations thereof.

33. (Previously Presented) The electrical structure of claim 42, wherein said one or more power supplies of voltage island V_X for X=1, 2,…, N are each independently coupled to one of (a) said one or more power supplies of voltage island V_Y, for Y=1, 2,…, N, X not equal to Y, (b) a VDDO power supply of said parent terrain or (c) one or more external to said parent terrain power supplies.

34. (Previously Presented) The method of claim 31, wherein each voltage island of the N voltage islands includes (a) an externally supplied VDDN power supply and a voltage shifting means, or (b) said externally supplied VDDN power supply and a fencing means, or (c) said externally supplied VDDN power supply, said voltage shifting means and said fencing means.

35. (Previously Presented) The method of claim 34, wherein said fencing means comprises logic latches.

36. (Previously Presented) The method of claim 34, wherein each voltage island of the N voltage islands further includes one or more substructures selected from the group consisting of (a) an internal voltage island VDDI power distribution network, (b) state saving means, (c) one or more switching elements coupled between said externally supplied VDDN power supply and said internal voltage island VDDI power distribution network, and (d) one or more voltage buffering circuits.

37. (Previously Presented) The method of claim 36, wherein said one or more switching elements is selected from the group consisting of hard connections, voltage regulators, headers and footers.

38. (Previously Presented) The method of claim 36, wherein said state saving means includes at least one state saving latch.

39. (Previously Presented) The electrical structure of claim 42, wherein one or more voltage islands of the N voltage islands further includes a power management state machine coupled to an internal voltage island VDDI power supply distribution network, said power management state machine of voltage island V_X for X=1, 2,..., N located in (a) a voltage island V_Y for Y=1, 2,..., N, Y less than X, or (b) in said parent terrain.

40. (Previously Presented) The method of claim 31, wherein said parent terrain is an integrated circuit chip or a voltage island within said integrated circuit chip.

41. (Previously Presented) The electrical structure of claim 21, further including:

additional voltage islands denoted as V_3, V_4,..., V_N, a voltage island V_Z nested within a voltage island V_{Z-1} for Z=3, 4,..., N, wherein N is an integer of at least 3.

42. (Currently Amended) The method of claim [[21]] 31, further including:

providing additional voltage islands denoted as V_3, V_4,..., V_N; and

nesting a voltage island V_Z within a voltage island V_{Z-1} for Z=3, 4,…, N, wherein N is an integer of at least 3.

43. (New) The electrical structure of claim 21, further including:

a fence-in circuit coupled to an input of said logic circuit, an output of said logic circuit coupled to an input of said state saving circuit; and

a fence out circuit coupled to an output of said state saving latch.

44. (New) The electrical structure of claim 43, further including:

an additional logic circuit coupled between said state saving latch and said fence-in circuit.

45. (New) The electrical structure of claim 43, further including:

a fencing power supply connected to said fence-in and said fence-out circuits.

46. (New) The method of claim 31, further including:

providing a fence-in circuit coupled to an input of said logic circuit, an output of said logic circuit coupled to an input of said state saving circuit; and

providing a fence out circuit coupled to an output of said state saving latch.

47. (New) The method of claim 46, further including providing an additional logic circuit coupled between said state saving latch and said fence-in circuit.

48. (New) The method of claim 46, further including:

providing a fencing power supply connected to said fence-in and said fence-out circuits.